

POSZ LAW GROUP, PLC

ATTORNEYS AT LAW

12040 SOUTH LAKES DRIVE, SUITE 101
RESTON, VA 20191

SPECIALIZING IN PATENTS, TRADEMARKS & COPYRIGHTS

DAVID G. POSZ
JAMES E. BARLOW *
BRIAN C. ALTMILLER
ROBERT L. SCOTT, II
CYNTHIA K. NICHOLSON* NOT ADMITTED IN VIRGINIA
PRACTICE LIMITED TO FEDERAL PATENT,
TRADEMARK AND COPYRIGHT MATTERSTEL: (703) 707-8110
FAX: (703) 707-8118
WWW.POSZLAW.COM**FACSIMILE TRANSMISSION**

Date: August 11, 2005

Pages: 4

To: **U.S. Patent Office -
Office of Finance - Refund Branch**
Fax No.: 571-273-8500

From: David G. Posz

Subject: **Request for Refund of IDS Fee**

Applicant(s): FUJITA et al.

Atty. Dkt.: 01-242

Serial No.: 10/022,794

Group Art Unit: 2152

Filed: December 20, 2001

Examiner: Unknown

Title: MICROCOMPUTER

Sirs,

Applicants request a refund to Deposit Account 50-1147 of the PTO fee of \$180 for the submission of Information Disclosure Statement which was charged to our Deposit Account 50-1147 on February 2, 2005 since the fee was not required for this application. The foreign communication was issued on October 26, 2004 (Heisei-16, Japanese Era of Heisei, which is A.D. 2004).

Copies of the Supplemental Information Disclosure Statement of December 9, 2004 and our Deposit Account Statement of February 2005 are attached herewith.

Authorization is hereby given to charge any fee deficiencies or credit any overpayment to Deposit Account 50-1147.

Respectfully submitted,


David G. Posz
Reg. No. 37,701

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): FUJITA et al.	Atty. Dkt.: 01-242
Serial No.: 10/022,794	Group Art Unit: 2152
Filed: December 20, 2001	Examiner: Unknown
Title: MICROCOMPUTER	

Commissioner for Patents
Arlington, VA 22202

Date: December 9, 2004

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the references listed on the attached Form PTO-1449 are being brought to the attention of the Examiner without any admission that they constitute statutory prior art, or without any admission that they contain subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

Further, pursuant to 37 C.F.R. §1.97(e), the undersigned hereby certifies that each listed reference was first cited in a Communication (copy enclosed) from a foreign patent office in connection with a counterpart foreign application not more than three months prior to the filing of this statement.

Although no fees are believed to be due at this time, it is respectfully requested that any such fees be charged to Deposit Account 50-1147. Also, the Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed references have been considered and made of record.

Respectfully submitted,



David G. Posz
Reg. No. 37,701

Posz & Bethards, PLC
11250 Roger Bacon Drive
Suite 10
Reston, VA 20190
(703) 707-9110 (phone)
Customer No. 23400

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PATENT APPLICATION
Page 1 of 1

FORM PTO-1449	ATTY. DKT NO.	01-242	SER. NO.	10/022,794
	APPLICANT	FUJITA et al.		
	FILING DATE	December 20, 2001	GROUP	2152

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

TRANSLATION

	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	NO
	JP-A-8-063451	03/08/96	JAPAN				Engl. Abstract	
	JP-A-64-059551	03/07/89	JAPAN				Engl. Abstract	
	JP-A-3-175518	07/30/91	JAPAN				Engl. Abstract	
	JP-A-9-114560	05/02/97	JAPAN				Engl. Abstract	
	JP-U-58-101233	07/09/83	JAPAN					X
	JP-A-64-88615	04/03/89	JAPAN				Engl. Abstract	

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at <http://www1.ipdl.jp.go.jp/PA1/cgi-bin/PA1INDEX>.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED	

Rev. 10/94 (Form 3.05)

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Date mailed: Heisei-16, October 26

The reason of rejection

Japanese patent application No.2000-402423

Rejection Date Heisei 16, October 21

The present inventions claimed in following claims are rejected under Japanese Patent Law §29 second paragraph over the publications described below.

[With regard to claim 1] Cited Publication 1

The cited publication 1 discloses " A microcomputer includes an automatic signal reading means (a revived input detecting circuit) for reading and determining a level of signal supplied to the predetermined input terminal when the CPU is in the stop condition, and then raising the CPU to the operating condition from the stop condition when the determined level reaches the particular level."

It is a design matter that reading and determining a level of signal supplied to the input terminal are executed every constant period.

[With regard to claim 2] Cited publications 1, 2

As to the cited publication 1, refer to [With regard to claim 1].

As disclosed in the cited publication 2, "In the input circuit, when the level of the input signal becomes identical continuously for a plurality of times, it is effective." is well known technique.

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Posz & Bethards, PLC
11250 Roger Bacon Drive
Suite 10
Reston, VA 20190
(703) 707-9110 (phone)
Customer No. 23400

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M. FL1005 180.00 SA

Adjustment Date: 10/04/2005 SDIRETA1
02/02/2005 FBRI SCDE 00000006 501147 10022794
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